CLAIMS

What is claimed is:

1. A circuit for correcting an offset of an amplification and low-pass filtering chain having a predetermined gain and a predetermined cut-off frequency depending on a value of at least one capacitor, the circuit comprising:

a correction means for subtracting from an input signal of the chain a correction signal depending on a value of a programmable digital word;

a digital automaton for, in a setting phase, searching, then memorizing one of two consecutive values of the digital word between which an output signal of the chain switches sign, the input signal being canceled during the setting phase; and

a means for, during the setting phase, reducing the value of said at least one capacitor with respect to its normal operating value.

2. The circuit of claim 1 wherein the means for reducing the value of said at least one capacitor includes a means for, during the setting phase, reducing the value of each capacitor with respect to its normal operating value.

3. The circuit of claim 1 wherein the means for reducing the value of said at least one capacitor includes a means for switching said at least one capacitor with a capacitor of value smaller than the normal operating value of said at least one capacitor.

4. The circuit of claim 1 wherein said at least one capacitor is formed of a capacitor of small value connected in parallel to a plurality of small capacitors each series-connected to a respective programmable switch, and wherein the means for reducing the value of said at least one capacitor is capable of controlling the turning-off of the programmable switches.

5. A method for correcting an offset of a chain of amplification and low-pass filtering of an input signal, having a predetermined gain and a predetermined cut-off frequency depending on a value of at least one capacitor, the method comprising:

a) canceling the input signal of the chain;

b) subtracting from the input signal of the chain a correction signal depending on a value of a digital word and modifying said value from a predetermined initial value to any one of two consecutive values between which an output signal of the chain switches sign; and

c) memorizing the value of the digital word;

wherein, during implementation of b), the value of said at least one capacitor is reduced with respect to its normal operating value to increase the cut-off frequency.

6. The method of claim 5 wherein reducing the value of said at least one capacitor includes, during a setting phase, reducing the value of each capacitor with respect to its normal operating value.

7. The method of claim 5 wherein reducing the value of said at least one capacitor includes switching said at least one capacitor with a capacitor of value smaller than a normal operating value of said at least one capacitor.

8. The method of claim 5 wherein reducing the value of said at least one capacitor includes using programmable switches to control that value.

9. An apparatus to correct an offset of a filter chain having at least one cut-off frequency that depends on a value of at least one capacitor, the apparatus comprising:

a setting element coupled to a filter in the filter chain to reduce, during a setting phase, the value of the at least one capacitor with respect to that capacitor's normal operating value.

10. The apparatus of claim 9 wherein the filter comprises:

an input terminal and an output terminal;

a resistor coupled between the input and output terminals of the filter; and

the capacitor having a first terminal coupled to the output terminal and a second terminal coupled to ground, wherein the setting element includes:

another capacitor of smaller value relative to the capacitor of the filter and having a first terminal coupled to the output terminal of the filter;

a first switch coupled between a second terminal of the another capacitor and ground; and

a second switch coupled between the second terminal of the capacitor of the filter and ground.

11. The apparatus of claim 10 wherein during normal operation, the first switch is off and the second switch is on, and wherein during the setting phase, the first switch is on and the second switch is off.

12. The apparatus of claim 9, further comprising:

a converter coupled to an input terminal of the filter chain to subtract, from an input signal to the filter chain, a correction signal that depends on a value of a programmable digital word;

an automaton to, in the setting phase, search and then memorize one of two consecutive values of the digital word between which an output signal of the filter chain switches sign; and

a switch coupled to the input terminal of the filter chain to cancel the input signal during the setting phase.

13. The apparatus of claim 9 wherein the filter includes:

a current input terminal and a voltage output terminal;

a first amplifier having an input terminal coupled to the current input terminal and having an output terminal;

a second amplifier having an input terminal coupled to the output terminal of the first amplifier and having an output terminal coupled to the voltage output terminal, the second amplifier further being coupled to a first capacitor in parallel to form an integrator assembly, the first capacitor having a first terminal coupled to the output terminal of the first amplifier;

a second capacitor and a first resistor coupled in parallel between the current input and voltage output terminals of the filter; and

a third capacitor and a second resistor coupled in parallel and coupled between the current input terminal of the filter and a voltage reference.

14. The apparatus of claim 13 wherein the setting element is coupled to the first capacitor and to the voltage output terminal of the filter to reduce a value of the first capacitor during the setting phase.

15. The apparatus of claim 14, further comprising:

a first additional setting element coupled to the second capacitor and to the voltage output terminal of the filter to reduce a value of the second capacitor during the setting phase; and

a second additional setting element coupled to the third capacitor and to the current input terminal of the filter to reduce a value of the third capacitor during the setting phase.

16. The apparatus of claim 15 wherein each of the setting elements includes:

an adjustment capacitor having a value that is smaller relative to a value of a capacitor to which the setting element is respectively coupled; and

at least one switch coupled to the adjustment capacitor to control reduction of the value of the capacitor to which the setting element is respectively coupled.

17. The apparatus of claim 16 wherein the at least one switch comprises a plurality of programmable switches.

18. A circuit to correct an offset of an amplification and low-pass filter chain having a predetermined gain and a predetermined cut-off frequency depending on a value of at least one capacitor, the circuit comprising:

a correction unit to subtract, from an input signal of the chain, a correction signal depending on a value of a programmable digital word;

a digital automaton unit coupled to the correction unit to, in a setting phase, search and then memorize one of two consecutive values of the digital word between which an output signal of the chain switches sign;

a switch coupled to the filter chain to cancel the input signal during the setting phase; and

at least one setting element coupled to the at least one capacitor to, during the setting phase, reduce a value of the at least one capacitor with respect to its normal operating value to increase the cut-off frequency.

19. The circuit of claim 18 wherein the at least one capacitor is part of a filter, the filter comprising:

an input terminal and an output terminal;

a resistor coupled between the input and output terminals of the filter; and

the at least one capacitor having a first terminal coupled to the output terminal and a second terminal coupled to ground, wherein the setting element includes:

another capacitor of smaller value relative to the at least one capacitor of the filter and having a first terminal coupled to the output terminal of the filter;

a first switch coupled between a second terminal of the another capacitor and ground; and

a second switch coupled between the second terminal of the capacitor of the filter and ground.

20. The circuit of claim 19 wherein during normal operation, the first switch is off and the second switch is on, and wherein during the setting phase, the first switch is on and the second switch is off.

21. The circuit of claim 19 wherein the first switch is a programmable switch.

22. The circuit of claim 19 wherein the filter chain includes a transresistance amplifier and an integrator assembly, the circuit further comprising a plurality of setting elements respectively coupled to capacitors of the transresistance amplifier and the integrator assembly to reduce a value of these capacitors during the setting phase.